A Switched-Current Slice of Cells for Adaptive Filters

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Abstract— **Simulation results of the interconnection of previously proposed switched-current (SI) cells are presented as a first step to the overall design of an analog adaptive filter. Two kinds of multipliers employing different techniques are tested, showing the usefulness of the difference integrator proposed. Due to the modularity presented by the filter structure a slice is first analyzed.**

I. Introduction

Due to its simplicity and convergence characteristics [1], the least-mean-squares (LMS) algorithm is usually applied to the implementation of adaptive filters. Switched-current (SI) cells were proposed in [2], aiming to investigate their applicability on SI LMS-based adaptive filter implementation. Design constraints were analyzed in [3]. Since we are dealing with analog design it is advisable to test some parts of the overall circuit before implementation. As the system intended for testing is highly modular, simulation results of a system slice are presented here. Design alternatives for the multipliers are considered. The main points addressed in the paper are as follows. Section II describes the system we aim to design. The cells of a system slice are presented in Section III. In Section IV, a summary of implementation details is presented. Finally, simulation results are presented in Section V.

II. Test system

In order to test the applicability of the SI cells presented in [2], the test system depicted in Fig. 1 will be used. It is a transversal finite impulse response (FIR) filter that uses the LMS adaptation algorithm. The system is defined by the following equations

$$\boldsymbol{x}(k) = [x(k), x(k-1), \ldots, x(k-N)]^T$$

$$\boldsymbol{w}(k) = [w_0(k), w_1(k), \ldots, w_N(k)]^T$$

$$y(k) = \boldsymbol{w}^T(k)\boldsymbol{x}(k)$$

$$e(k) = d(k) - y(k)$$

$$\boldsymbol{w}(k+1) = \boldsymbol{w}(k) + 2\mu e(k)\boldsymbol{x}(k)$$

where $x(k)$ is the input signal, $\boldsymbol{w}(k)$ is the weight (coefficient) vector, $y(k)$ is the output signal, $d(k)$ is the reference signal and $e(k)$ is the error signal.

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III. Implemented slice

For testing cells interconnection, the system slice showed in Fig. 2 was implemented. The following cells were needed: unit delay, multiplier and integrator.

The unit delay is composed by two of the switched regulated cascode (SRC) memory cell (MC) illustrated in Fig. 3. Cascode current sources were used. The simplified unit delay, as well as the switching scheme, are depicted in Fig. 4.

The multiplier and the multiplier-integrator cells proposed in [2] have a drawback. They need the input currents to be stable during a switching period. If we consider that these cells and the unit delay are in series, the global switching frequency will be three times lower than that of the cells. The simplest solution was to substitute the switched multiplier by a continuous-time one. The first continuous-time multiplier (MULT1) considered was the one also proposed, but not implemented, in [2]. It is shown in Fig. 5 and the multiplication is done on basis of add/subtract operations that eliminate square and offset components. Depending on how the currents i_1 to i_4 are combined, other circuits can be obtained, as the one in Fig. 6. Aiming to reduce the area occupied, the multiplier (MULT2) proposed in [4] and illustrated in Fig. 7 was tried too. It consists on two current squarer modules and a subtraction mirror, that implement the quarter-square technique.

The SI multiplier-integrator cell in [2] uses an add-subtract-accumulate module to perform the operations needed by MULT1. Another SI multiplier-integrator can be implemented, as in Figs. 8 and 9, using the squarer cell of MULT2 and the difference integrator cell of MULT1 to perform the quarter-square operation. That shows the usefulness of the difference-integrator cell proposed in [2]. Superscripts in some of the currents denote clock phase.

A multiplier employing square components elimination and using the squarer cell mentioned above, but that is different from MULT1 and MULT2, was proposed in [5].

IV. Implementation details

This section summarizes some details that have been taken into account in the design of the filter slice illustrated in Fig. 10.

The switches are n-type MOS transistors.

All the n-type transistors in the memory cell have the substrate (bulk) terminal tied to the V_{SS} power supply.

On implementing the taps of the delay line both the $\frac{W}{L}$ ratio and the storage capacitor of the transistor M1 in Fig. 3 were preserved through the replication circuit. From Fig. 11 that means: $WL = \sum_{i=1}^{N} k_i W_i L_i$ and $\frac{W}{L} = \frac{W_1}{L_1}$.

The negative taps were obtained by using the cascode current inverter shown in Fig. 12.

During some phases, the input current i_S and the output current of some of the delay taps are not used. In order to sink them in the right way, an extra power supply V_{SINK} and some extra switches, as well as their switching signals, are included.

The current squarer cell was implemented using p-type transistors aiming to keep the source and substrate (bulk) terminals connected together.

V. Simulation results

Simulation results are presented from: i) a delay line with two unit delays, ii) the multipliers MULT1 and MULT2, and iii) the whole slice.

A clock sequence similar to the one in Fig. 4 was used, starting with a reset arrangement, in order to have the correct initial conditions. During a sample-and-hold period of the multiplier-integrator, the delay line is put on hold state and vice-versa. The simulations were performed using $V_{DD} = -V_{SS} = 3.5V$ for the multiplier MULT1 and $V_{DD} = 7V$ and $V_{SS} = 0V$ for the other cells. The memory cell was designed for a maximum input current of $40\mu A$, over bias currents of $I_P = 100\mu A$ and $bI_P = 10\mu A$. The squarer and the multiplier MULT2 cells work under $2I_B = 34\mu A$. The inverter cell bias (V_{BRH} and V_{BRL}) comes from the memory cell current source (I_p).

The delay was driven with a triangular shape current with $f_{tg} = 71.43kHz$ and $i_{tg} = \pm 60\mu A$, switched at $f_{ck} = 1.04MHz$ and $V_{ck} = 7V$. A DC sweep was performed for both the multipliers. The input current i_E was increased from $-20\mu A$ to $20\mu A$ (step $4\mu A$) for MULT1 and from $-30\mu A$ to $30\mu A$ (step $5\mu A$) for MULT2. The slice had an input current of $i_S = 20\mu A$ and a feedback current $i_F = 10\mu A$ applied to it.

Fig. 13 shows the input signal as well as the output current of both delay cells in the delay line. Figs. 14 and 15 present the theoretical and simulated DC sweeps for the multipliers MULT1 and MULT2, respectively. Fig. 16 depicts the integrator current as well as its tap. The slice output current, that is the multiplier output current, can be seen in Fig. 17. The negative peaks in this curve are due to switching in the delay line. The effects of charge injection in the SRC memory cell matched those ones found in [6]. They are of the order of $\Delta I = 0.1\mu A$ for a memory cell which has a settling time of $t_{st} = 20ns$, switched at $V_{ck} = 7V$ within $t_{rise/fall} = 40ns$.

VI. Conclusion

Aiming an SI implementation for a LMS-based adaptive filter, some SI cells were presented previously. This work put them together in a slice of the whole system. Two alternatives for the multiplier were presented, showing the usefulness of the difference-integrator cell proposed. Some implementation details and interconnection constraints were also discussed. Some simulation results were presented, which show that the cells work as expected. Future work will investigate how to improve the performance of the cells and propose a more efficient system switching scheme.

References

[1] P. S. R. Diniz. *Adaptive Filtering: Algorithms and Practical Implementation.* Kluwer Academic Publisher, Boston, MA, 1997.

[2] Alexandre S. de la Vega, Antônio C. M. de Queiroz, and Paulo S. R. Diniz. New switched-current cells for adaptive filters. *Proc. IEEE ISCAS*, 1997.

[3] Alexandre S. de la Vega, Antônio C. M. de Queiroz, and Paulo S. R. Diniz. On the implementation of switched-current cells for adaptive filters. *Proc. of the First International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, 1997.

[4] K. Bult. *Analog CMOS Square-Law Circuits.* PhD thesis, University of Twente, Enschede, The Netherlands, 1988.

[5] G. H. M. Joordens, J. A. Hegt, and D. M. W. Leenaerts. A high performance low voltage switched-current multiplier. *Proc. IEEE ISCAS*, 3:1856–1859, 1995.

[6] N. C. Battersby. *Switched-Current Techniques for Analogue Sampled-Data Signal Processing.* PhD thesis, University of London, London, 1993.

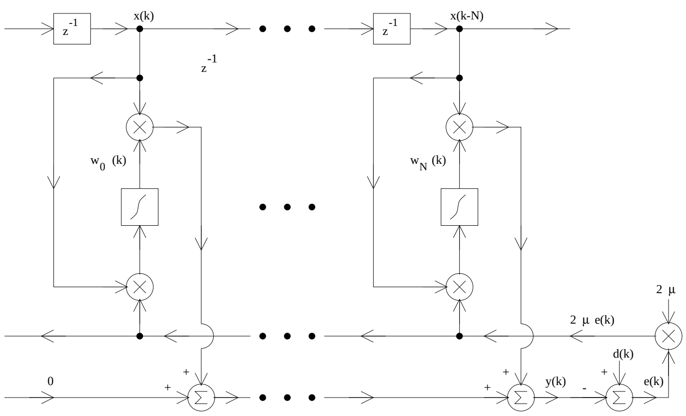

Fig. 1. Test system.

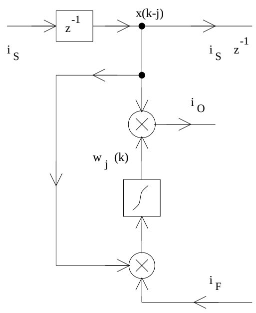

Fig. 2. Implemented slice.

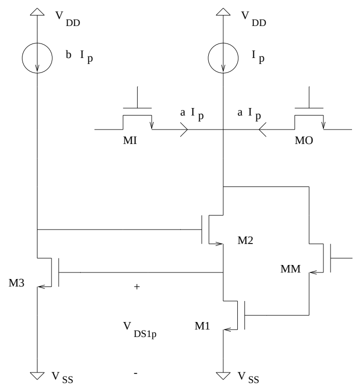

Fig. 3. Memory cell structure.

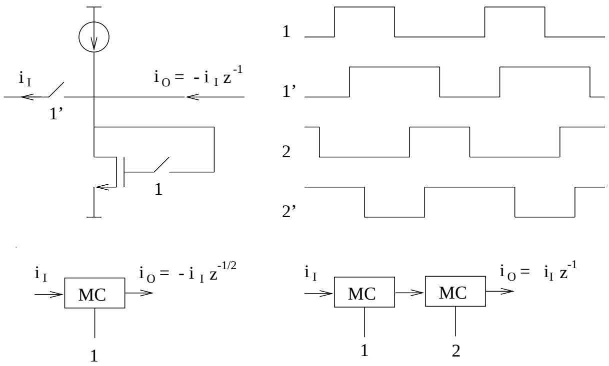

Fig. 4. SI delay cells.

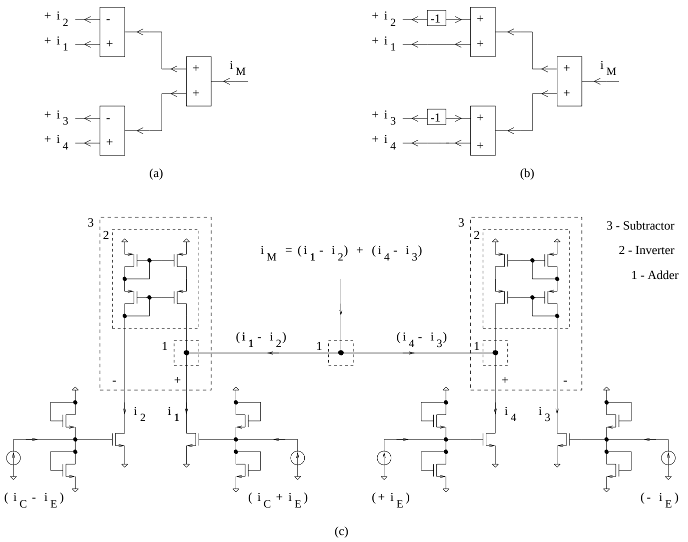

Fig. 5. Continuous-time multiplier 1.

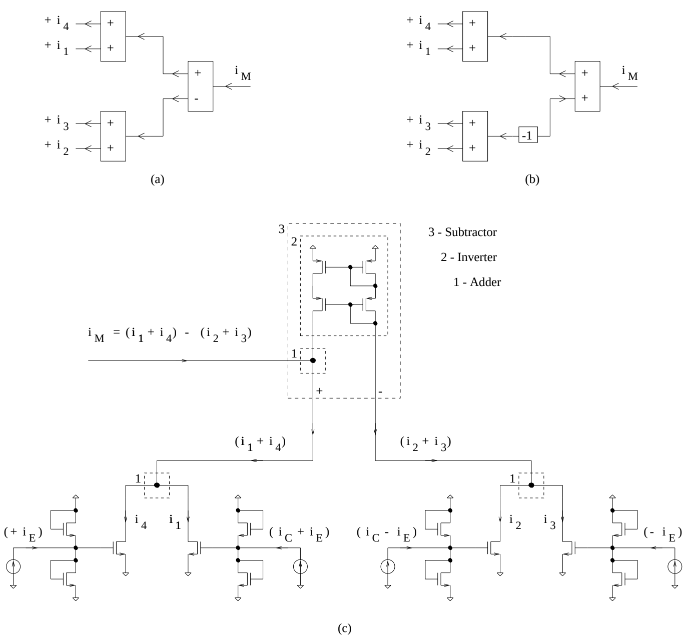

Fig. 6. Continuous-time multiplier 1b.

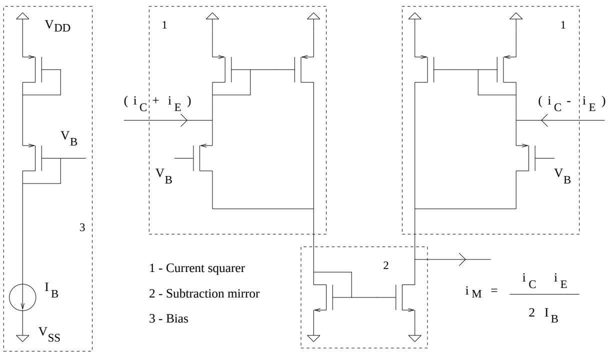

Fig. 7. Continuous-time multiplier 2.

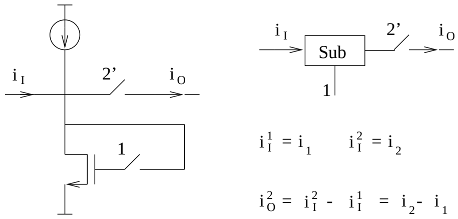

Fig. 8. SI subtractor.

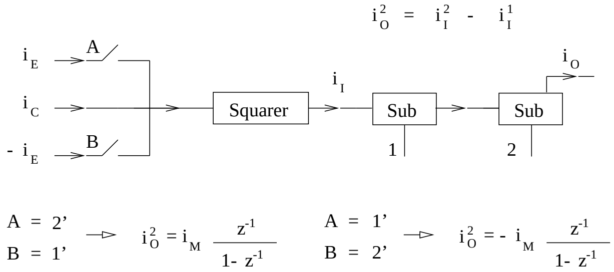

Fig. 9. SI multiplier-integrator 2.

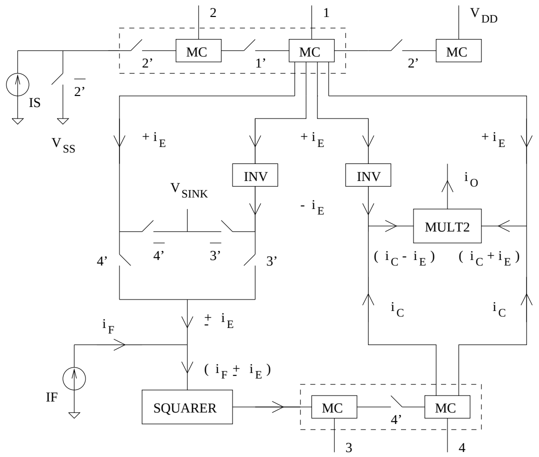

Fig. 10. Filter slice (schematics).

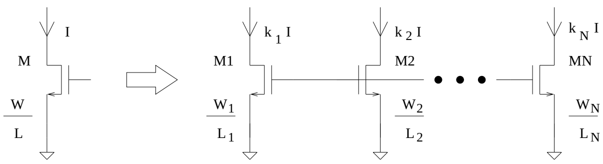

Fig. 11. Current replication.

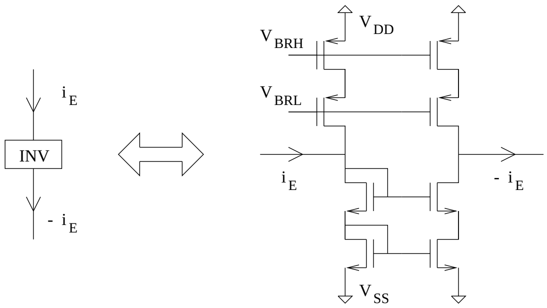

Fig. 12. Cascode current inverter.

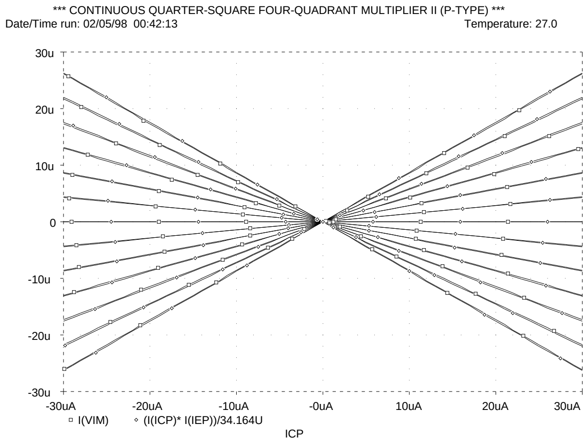

Fig. 15. Simulation results (multiplier MULT2).

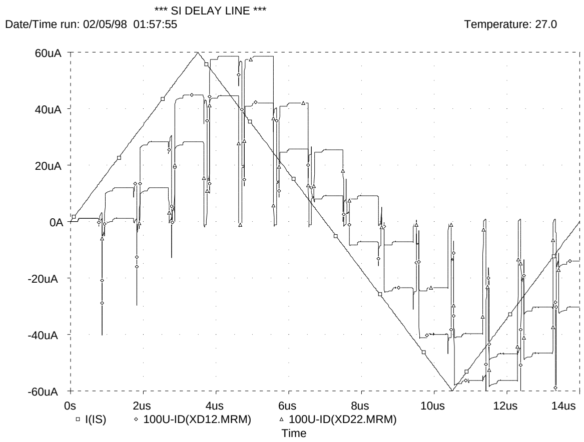

Fig. 13. Simulation results (delay line).

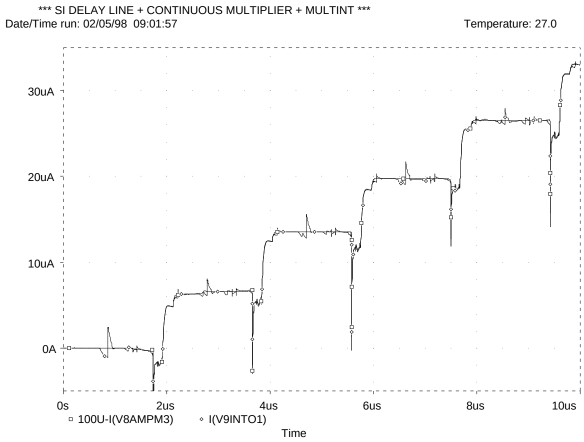

Fig. 16. Simulation results (multiplier-integrator).

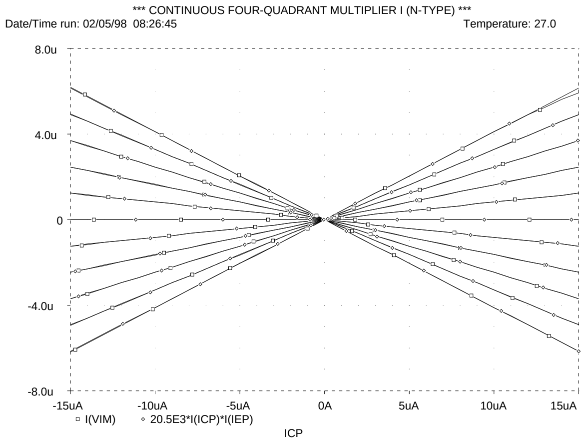

Fig. 14. Simulation results (multiplier MULT1).

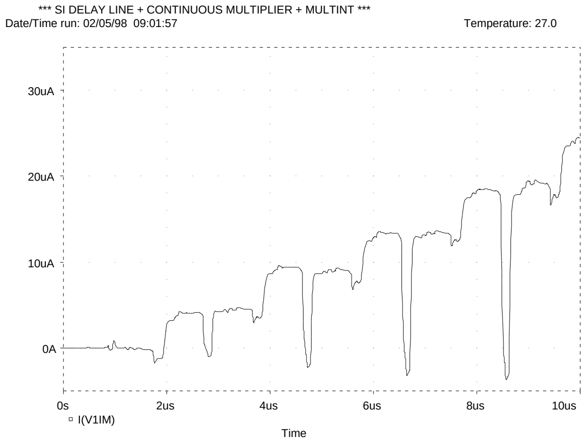

Fig. 17. Simulation results (multiplier).