# New Switched-Current Cells for Adaptive Filters

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*Abstract*— ***A family of continuous-time and switched-current (SI) four-quadrant current-multipliers are proposed, based on a current-gain cell linearly controlled by a current, as well as an SI version of that cell. The use of a subtractor is also proposed, which eliminates current offsets. Based on this property an offset-free four-quadrant multiplier-integrator cell is also presented. The new circuits are meant to implement adaptive filters.***

## I. Introduction

The least-mean-squares (LMS) algorithm is largely used in adaptive filtering due to its simplicity and convergence characteristics [1]. To implement these filters, blocks such as delays, adders, multipliers, integrators and variable gain cells are needed. Analog [2], [3], [4] and digital implementations are found in the literature, and, recently, a switched-capacitor adaptive filter [5] has been proposed. The switched-current (SI) technique [6], [7] has been used in a variety of designs and an SI current multiplier was proposed in [8]. Despite of that, no SI-based adaptive filter has been proposed. In order to investigate the feasibility of implementing an SI LMS-based adaptive filter, some cells are proposed in this work, which are made from two basic cells and have practically the same structure. Also, an offset-free multiplier-integrator cell is found, what is an interesting result, since offset is a major concern in the implementation of adaptive filters [9]. The main points addressed in the paper are as follows. Section II presents a review of the previously proposed gain cell [10]. The multiplier equations that we propose, as well as an extension of the previous gain equations [10], are derived in Section III. In Section IV, a continuous-time four-quadrant current multiplier is advanced. Some SI cells are proposed in Section V. Finally, simulation results are presented in Section VI.

## II. Previous current-gain cell

The current-gain cell first presented in [10] can be seen in Figs. 1 and 2. The A/S block implements an add-and-subtraction operation between the currents $I_C$ and $I_E$ by means of a sequence of biased current mirrors. The I-V block implements a linear resistor [11] and the V-I block is a simple transconductor (one transistor) using the quadratic law to generate the output current. Considering all transistors in saturation ($K = \mu C_{ox}\frac{W}{L}$ and $i_D = \frac{K}{2}(v_{GS} - V_T)^2$), the linear resistor (R) and the output current ($I_O$) are given by

$$R = \frac{1}{2K_3(V_{DD} - V_{T_3})} \tag{1}$$

$$I_O = (I_1 - I_2) = 2K_1R(RI_C - V_T)I_E \tag{2}$$

Equations (1) and (2) apply for symmetrical power supplies ($V_{DD} = -V_{SS}$). For single power supply ($V_{SS} = 0$) the equations are

$$R' = \frac{1}{2K_3(\frac{V_{DD}}{2} - V_{T_3})} \tag{3}$$

$$I'_O = (I'_1 - I'_2) = 2K_1R'(\frac{V_{DD}}{2} + R'I_C - V_T)I_E \tag{4}$$

where $\mu$ is the mobility of the carriers, $C_{ox}$ is the gate capacitance per unit area, $V_T$ is the threshold voltage, $W$ and $L$ are the channel width and length, respectively, and $V_{DD}$ and $V_{SS}$ are the power supplies.

## III. Multiplier equations

A four-quadrant current-multiplier can be implemented using the same idea of the gain cell described above [10], as will be shown. The basic equations for the multiplier and the extension for the gain cell equations are first derived. Then, some design equations are obtained and are listed in the following.

### A. Basic equations

The linear resistor can be powered by single or dual power supply. Under dual power supply, the control current $I_C$ must be unipolar, while the input current $I_E$ can be bipolar. Adding an additional bias current $I_{B_C}$ to the input current $I_C$, both input currents ($I_C$ and $I_E$) can be bipolar, and the multiplication is obtained by

$$\begin{aligned} i_{O_{12}} &= (i_1 - i_2) = 2K_1R[R(I_{B_C} + i_C) - V_T]i_E \\ &= (2K_1R^2)i_Ci_E + 2K_1R(RI_{B_C} - V_T)i_E \end{aligned} \tag{5}$$

$$i_{O_{34}} = (i_3 - i_4) = 2K_1R(RI_{B_C} - V_T)i_E \tag{6}$$

$$i_M = (i_{O_{12}} - i_{O_{34}}) = (2K_1R^2)i_Ci_E \tag{7}$$

For a single power supply, equation (4) shows that the resistor itself can bias the transconductor, directly allowing bipolar input currents ($i_C$ and $i_E$). In this case, the equations are

$$\begin{aligned} i_{O_{12}} &= (i_1 - i_2) = 2K_1R'(\tfrac{V_{DD}}{2} + R'i_C - V_T)i_E \\ &= (2K_1R'^2)i_Ci_E + 2K_1R'(\tfrac{V_{DD}}{2} - V_T)i_E \end{aligned} \tag{8}$$

$$i_{O_{34}} = (i_3 - i_4) = 2K_1R'(\frac{V_{DD}}{2} - V_T)i_E \tag{9}$$

$$i_M = (i_{O_{12}} - i_{O_{34}}) = (2K_1R'^2)i_Ci_E \tag{10}$$

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An extension for equations (1)-(4) can be found by noting that the source terminals of the output transistors (M1 and M2) have not to be grounded, as in the gain cell of [10]. If they are tied to a $-V_{SS}$ power supply instead, equations (5)-(10) will hold if $V_T$ is changed to $V_T' = (-V_{SS} + V_T)$. Here again the additional bias current ($I_{B_C}$) can be avoided. In any case, a second output current $i_{O_{34}}$, that depends on $i_E$ only, has to be generated and subtracted from the original output current $i_{O_{12}}$ in order to produce the multiplier output current $i_M$. The building blocks implementing the equations (5)-(10) are depicted in Fig. 3. Several implementations can be derived as described in the next sections.

### B. Design equations

A further observation of equations (5)-(10) reveals that four currents ($i_1$, $i_2$, $i_3$, $i_4$) have to be generated and correctly added/subtracted in order to produce the output current ($i_M = i_1 - i_2 - i_3 + i_4$). Depending on the way those currents are combined, many implementations are possible. Equation (11) presents some examples.

$$\begin{aligned} (i_1 - i_2) - (i_3 - i_4) &= (i_1 - i_2) + (i_4 - i_3) = \\ -(i_2 - i_1) - (i_3 - i_4) &= -(i_2 - i_1) + (i_4 - i_3) \end{aligned} \tag{11}$$

A total of 48 equations (24 for $i_M$ and 24 for $-i_M$) similar to those ones in equation (11) can be obtained. At the time this paper was written, several implementations were found by the authors but, due to the lack of space, only some of them will be covered in the next sections. Some others will be reported later.

## IV. Continuous-time multiplier

As can be seen in Fig. 3, a continuous-time multiplier can be implemented by duplicating the gain cell of [10], applying to the second one only the current $i_E$ ($i_C = 0$), and combining the four currents to obtain $i_M$. The output current $i_M$ will suffer from mismatch effects, as in the gain cell of [10]. There, $I_O$ presents gain error and offset due to mismatches in $K_1$, $R$, and $V_T$ and nonlinearity distortion due to mismatches in $K_1$ and $R$. The way the four currents are combined can reduce the errors. In order to reduce both the area and the mismatches, a switched-current implementation can be used.

## V. Switched-current cells

The needed blocks for the LMS-based adaptive filter can be implemented using SI technique [6]. Some implementations will be covered here. Some others will be reported later. The basic block for such a design is the SI second-generation memory cell [6], [7], illustrated in Fig. 4. It should be noted that in SI design copies and negative values of the currents are usually available. Two basic cells are first defined which will be used to derive the other ones. Different clock sequences can generate not only a negative output current but modify the function performed by the cells. Superscripts in the currents denote clock phases.

### A. SI subtractor

Using the SI memory cell of Fig. 4 as a matched-inverter and accumulator, an SI subtractor can be implemented as proposed in Fig. 5.

### B. Switched gain-cell and switched I-V-I converters

Switched versions for the gain cell of [10] and the I-V-I converter are proposed in Figs. 6 and 7.

### C. SI gain cell

An SI version for the complete current-gain cell is proposed in Fig. 8. Since only one I-V-I converter is used, mismatches are avoided.

### D. SI four-quadrant multipliers

Two SI four-quadrant multipliers are proposed in Fig. 9. The first one employs two I-V-I converters and a single SI subtractor. It reduces mismatches by using half of the converters of that one in Fig. 3. The second one requires a single I-V-I converter and two SI subtractors. By using only one converter, mismatch effects are eliminated. The subtractors remove any offset from the output current. This is an important result which will be used below.

### E. SI difference integrator

From the series connection of two SI subtractors, a special SI integrator can be implemented, as illustrated in Fig. 10. Removing the passing switch, the resulting block will integrate the difference in the output current between the two phases. Assuming that a constant-offset current is present at the input for both phases, such a modified integrator will reject it. The same cell can be obtained from the usual SI integrator [6], by removing its input switch.

### F. SI multiplier-integrator

Finally, SI multiplier-integrator cells can be implemented as in Fig. 11. These cells are very similar to the proposed SI multipliers of Fig. 9.

## VI. Simulation results

The first multiplier of Fig. 9 and the first multiplier-integrator of Fig. 11 were simulated, as depicted in Fig. 12. The simulations were performed under $V_{DD} = -V_{SS} = 3.5V$, employing a clock sequence similar to the one in Fig. 4, at $f_{ck} = 5kHz$ and $V_{ck} = \pm 3.5V$. The switches are N-type MOS transistors. The memory cells are of switched regulated cascode type (SRC), biased by cascode current mirrors, as illustrated in Fig. 13. Assuming saturation, a maximum input current of $50\mu A$ is allowed. As shown in Fig. 14, the I-V-I converter is tied to $-V_{SS}$ and a negative $I_{B_C}$ is used to keep its output current within the dynamic range of the memory cell. The multiplier-integrator was driven by constant currents $i_E = 2\mu A$ and $i_C = 3\mu A$. The result can be visualized in Fig. 15. The effects of charge injection in the SRC memory cell matched those ones found in [6] and are of the order of $\Delta I = 0.2\mu A$. Better results can be achieved if other types of memory cell [6] and/or switching schemes to reduce charge injection and glitching [12] are used.

## VII. Conclusion

Aiming an SI implementation for a LMS-based adaptive filter, some continuous-time and SI cells were derived from the current-controlled current-gain cell of [10]. By duplicating the mentioned cell, a continuous-time four-quadrant multiplier was advanced. In order to minimize both the area and the mismatches, an SI design was tried. An SI subtractor was proposed from the usual SI memory cell [6] and switched versions for both the gain cell and the I-V-I converter were proposed. Using only those two blocks, an SI version for the gain cell, a four-quadrant multiplier, a difference integrator and a four-quadrant multiplier-integrator were proposed. Only some examples from a variety of possible implementations were presented. It should be noted that all the circuits are made from the same basic cells, some of them present similar structures, and changes in the clock sequences modify the operation of some cells. Simulation results show that, for the SI cells, the primary error source is charge injection in the memory switches, as expected. A more accurate analysis of the mismatch effects is under preparation.

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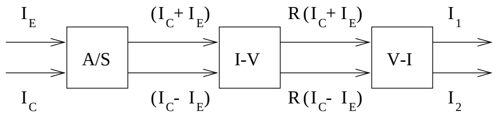


Fig. 1. Previous gain cell (schematics)

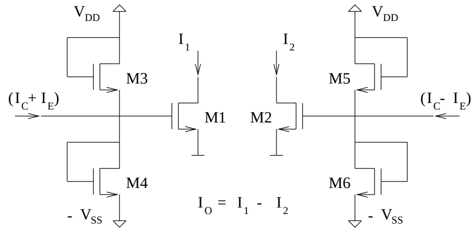


Fig. 2. Previous gain cell (circuit without the A/S block)

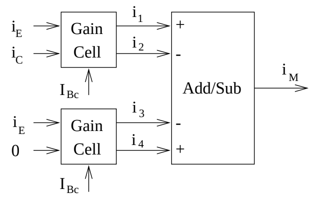


Fig. 3. Proposed continuous-time multiplier (schematics)

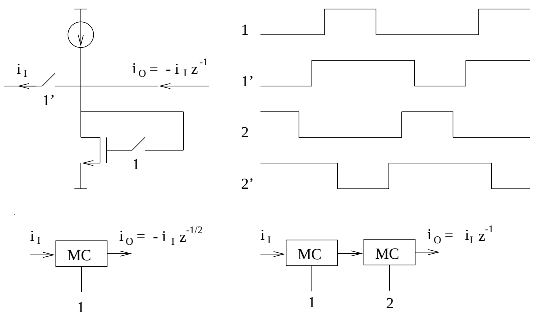


Fig. 4. SI memory cell

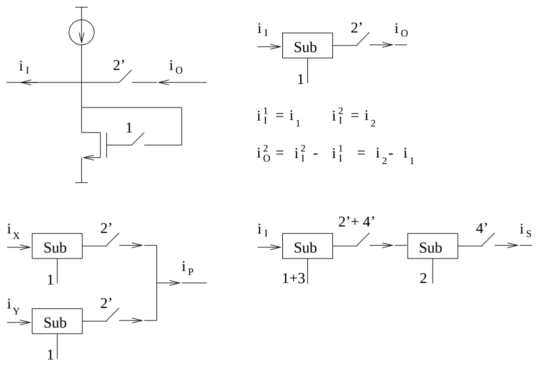


Fig. 5. Proposed SI subtractors

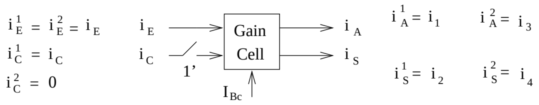


Fig. 6. Proposed switched gain cell

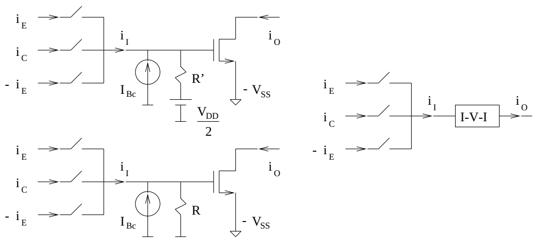


Fig. 7. Proposed switched I-V-I converters

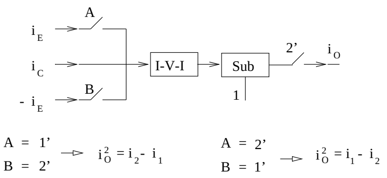


Fig. 8. Proposed SI gain cell

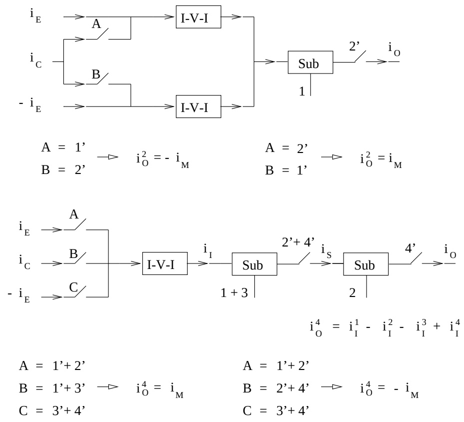


Fig. 9. Proposed SI four-quadrant multipliers

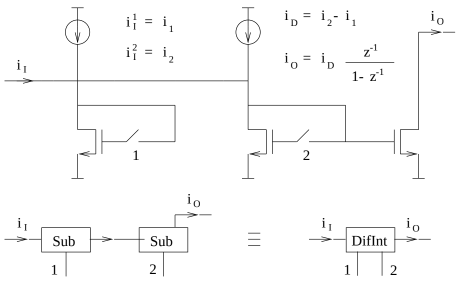


Fig. 10. Proposed SI difference integrator

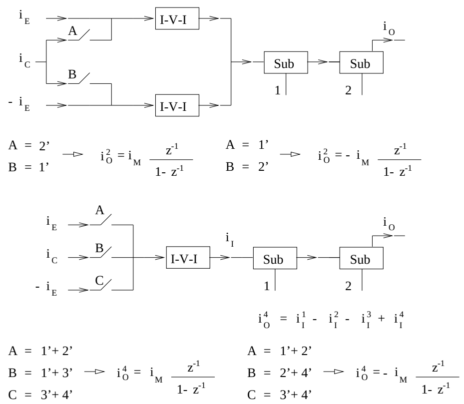


Fig. 11. Proposed SI multiplier-integrator cells

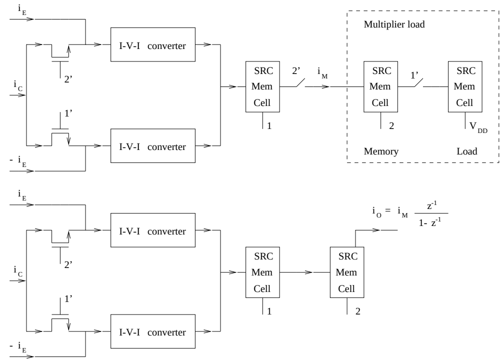


Fig. 12. Simulated SI multiplier and multiplier-integrator

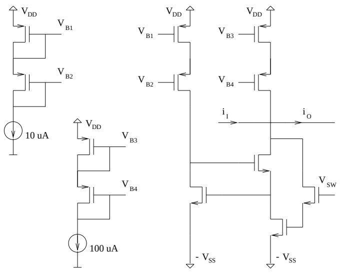


Fig. 13. Simulated SRC memory cell

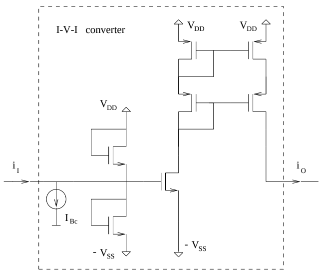


Fig. 14. Simulated I-V-I converter

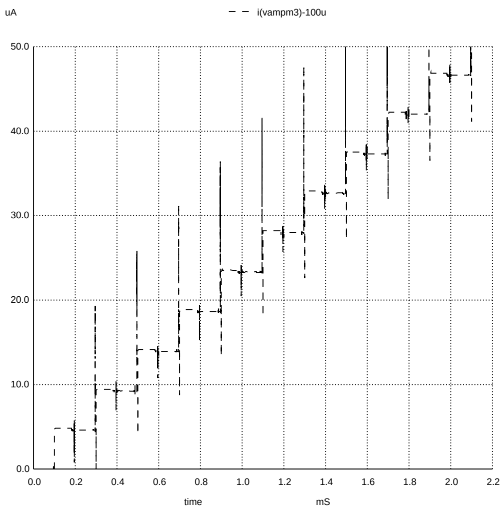


Fig. 15. Simulation results (multiplier-integrator)