On the Implementation of Switched-Current Cells for Adaptive Filters

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Abstract— **Implementation details of previously proposed switched-current (SI) cells are presented in order to obtain some guidelines for their design. Constraints related to the interconnection of the SI cells are also considered. Some simulation results are presented in order to verify the performance of the proposed cells. The new circuits are meant to implement adaptive filters.**

I. Introduction

The least-mean-squares (LMS) algorithm is widely used in adaptive filtering due to its simplicity and convergence characteristics [1]. To implement these filters, blocks such as delays, adders, subtractors, multipliers and integrators are needed. Analog [2], [3], [4] and digital implementations are found in the literature, and, recently, a switched-capacitor adaptive filter [5] has been proposed. The switched-current (SI) technique [6], [7] has been used in a variety of designs. Some SI cells were proposed in [8] aiming to investigate their applicability on SI LMS-based adaptive filters implementation. These cells were presented and analyzed as isolated blocks. Some care has to be taken on composing a system based on them. This work summarizes some implementation details that are important for the SI cells design and their interconnection, as well as presents some simulation results. The main points addressed in the paper are as follows. Section II describes the complete system we aim to design. The SI cells are presented in Section III. In Section IV, a summary of implementation details is presented. Finally, simulation results are presented in Section V.

II. Test system

In order to test the interconnection of the SI cells presented in [8] a test system must be first defined. Due to its simplicity, a system composed by a transversal finite impulse response (FIR) filter and the LMS adaptation algorithm was chosen. Such a system is depicted in Fig. 1 and its equations are listed below

$$\boldsymbol{x}(k) = [x(k), x(k-1), \ldots, x(k-N)]^T$$

$$\boldsymbol{w}(k) = [w_0(k), w_1(k), \ldots, w_N(k)]^T$$

$$y(k) = \boldsymbol{x}(k)\boldsymbol{w}^T(k)$$

$$e(k) = d(k) - y(k)$$

$$\boldsymbol{w}(k+1) = \boldsymbol{w}(k) + 2\mu e(k)\boldsymbol{x}(k)$$

where $x(k)$ is the input signal, $\boldsymbol{w}(k)$ is the weight (coefficient) vector, $y(k)$ is the output signal, $d(k)$ is the reference signal and $e(k)$ is the error signal.

To implement the test system the following cells are needed: unit delay, multiplier, integrator, adder and subtractor.

III. SI cells

The SI cells proposed in [8] are illustrated in Figs. 2-7. Most of them employ a two-phase clock scheme. Superscripts in some of the currents denote clock phase.

The start point is the memory cell. The switched regulated cascode (SRC) structure shown in Fig. 2 was used for testing. The unit delay, as well as a switching scheme, are depicted in Fig. 3. The subtractor and its series and parallel interconnections are shown in Fig. 4. In Figs. 5-6 the multiplier and the multiplier-integrator cells are depicted. Two of the nonlinear I-V-I converter used by the multiplier type cells can be seen in Fig. 7, which shows a gain cell previously presented in [9]. Transistors M3-M4 (M5-M6) implement a linear resistor and M1 (M2) is a nonlinear transconductor.

IV. Implementation details

This section summarizes some implementation details that give some guidelines to the design of the SI cells and their interconnections.

A. RESET signal

In order to have the correct initial conditions, a RESET signal must be supplied to the cells. This is useful to: i) guarantee the correct bias of the memory cells, ii) avoid different values between current sources and sinks and iii) apply zero initial conditions to the integrator cells.

B. Switching signals

A special care has to be taken on defining the switching signals. The sequence has to guarantee that the sum of the currents is always correct. For instance, the switching signals in Fig. 3 are correct for a delay line. But they can be a problem for the multiplier-integrator cells, since currents are changed during the hold phase of the memory cells. An alternative switching sequence can be found in Fig. 8, where passing switches are operated during the sample phase.

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C. Transistor dimensions

Transistor dimensions (width W and length L) in the memory cell of Fig. 2 are influenced by some conflicting parameters: settling time, dynamic range, storage error, bias currents, bias voltages and power supply. Even though it depends on the fabrication process parameters, it can be shown that the $\frac{W}{L}$ ratio of transistors M1-M3 can raise considerably with some combinations of dynamic range, bias currents and bias voltage of the drain of M1. The WL product of transistor M1 defines the parasitic storage capacitor. Defining high values for the WL product leads to low values for the storage error and high values for the settling time. Transistor dimensions of the current sources can be reduced if the power supply voltage is raised, increasing the power consumption.

D. Output current replication

Output current replication is useful not only to produce copies of the output currents but also to couple different current ranges by amplitude conditioning. It also imposes some rules on the dimensions of the transistor M1 in Fig. 2 and its associated mirrors, as shown in Fig. 9. Both the $\frac{W}{L}$ ratio and the storage capacitor has to be preserved through the replication circuit. That means: $WL = \sum_{i=1}^{N} k_i W_i L_i$ and $\frac{W}{L} = \frac{W_1}{L_1}$.

E. I-V-I converter

An extra degree of freedom in the design of the I-V-I converter is achieved by adding an output mirror to it, as can be seen in Fig. 10. The mirror couples the current ranges of the transconductor and the next cell. The following design equations can be obtained from Figs. 10 and 11. The output current is given by

$$i_0 \leq i_{MAX} \tag{1}$$

$$i_{01} + i_{02} = ni_0 \tag{2}$$

Considering that the next section is a memory cell, I_p is the bias current and a is the dynamic range, it follows that

$$i_{MAX} = aI_p \tag{3}$$

Considering all transistors in saturation and that μ is the mobility of the carriers, C_{ox} is the gate capacitance per unit area, V_T is the threshold voltage, W and L are the channel width and length, respectively, and V_{DD} and V_{SS} are the power supplies, their currents are given by

$$KP = \mu C_{ox}$$

$$i_D = \frac{KP}{2}\frac{W}{L}(v_{GS} - V_T)^2$$

$$i_{01} = \frac{KP}{2}\frac{W_1}{L_1}(v_{G1} + V_S - V_T)^2 \tag{4}$$

$$i_{02} = \frac{KP}{2}\frac{W_1}{L_1}(v_{G2} + V_S - V_T)^2 \tag{5}$$

From (1)-(5), it can be found that

$$[v_{G1} + (V_S - V_T)]^2 + [v_{G2} + (V_S - V_T)]^2 \leq \frac{naI_p}{\frac{KP}{2}\frac{W_1}{L_1}} \tag{6}$$

The voltage v_G and the linear resistor are defined by [10]

$$R = \begin{cases} \frac{1}{2KP\frac{W_3}{L_3}(V_{DD} - V_T)} & , \quad V_{DD} = V_{SS} \\ \frac{1}{2KP\frac{W_3}{L_3}(\frac{V_{DD}}{2} - V_T)} & , \quad V_{SS} = 0 \end{cases} \tag{7}$$

$$v_G = \begin{cases} Ri_R & , \quad V_{DD} = V_{SS} \\ Ri_R + \frac{V_{DD}}{2} & , \quad V_{SS} = 0 \end{cases} \tag{8}$$

For $V_{DD} = V_{SS}$, it follows that

$$(-V_{SS} + V_T) \leq (v_G = Ri_R) \leq (V_{DD} - V_T) \tag{9}$$

For $V_{SS} = 0$, equation (9) changes to

$$(V_T) \leq (v_G = Ri_R + \frac{V_{DD}}{2}) \leq (V_{DD} - V_T) \tag{10}$$

From (9)-(10), it can be deduced that

$$|i_R| \leq \begin{cases} \frac{V_{DD} - V_T}{R} & , \quad V_{DD} = V_{SS} \\ \frac{\frac{V_{DD}}{2} - V_T}{R} & , \quad V_{SS} = 0 \end{cases} \tag{11}$$

Equations (6)-(8) and (11) set the limits for the transistors dimensions in the I-V-I converters.

F. Cells interconnection

As isolated cells, most of the SI cells can work on a two-phase switching scheme. This may not be possible when these cells are interconnected. The primary problem is that both the multiplier and the multiplier-integrator cells need the same input currents during both the phases.

V. Simulation results

A delay line with two unit delays, the first multiplier of Fig. 5, and the first multiplier-integrator of Fig. 6 were simulated. The first two had a memory cell in the sample state as a load. In all of them, output current replication was applied. The simulations were performed using $V_{DD} = V_{SS} = 3.5V$. A clock sequence similar to the one in Fig. 8 was used, with $f_{ck} = 7kHz$ and $V_{ck} = \pm 3.5V$, and starting with a reset arrangement. The switches are N-type MOS transistors. The memory cells are of SRC type, biased by cascode current mirrors. The memory cell was designed for a maximum input current of $40\mu A$, over a bias current of $100\mu A$. The delay was driven with a triangular shape current with $f_{tg} = 357Hz$ and $i_{tg} = \pm 60\mu A$. A pulsed signal of $i_C = (3, 0, -3)\mu A$ and a constant current of $i_E = 2\mu A$ were supplied to the multiplier. The multiplier-integrator was driven by constant currents $i_C = 3\mu A$ and $i_E = 2\mu A$. Fig. 12 shows the input signal and output current of the first and forth memory cell of the delay line. Figs. 13 and 14 depicts only the output currents of the other cells. The effects of charge injection in the SRC memory cell matched those ones found in [6]. They are of the order of $\Delta I = 0.2\mu A$ and $\Delta I = 1.2\mu A$ for a settling time of $t_{st} = 2\mu s$ and $t_{st} = 0.1\mu s$, respectively.

VI. Conclusion

Aiming an SI implementation for a LMS-based adaptive filter, some SI cells were presented previously. This work summarizes implementation details and interconnection constraints that are important on building a system from those cells. Some simulation results were presented, which show that the cells work as expected. Future work will investigate how to improve the performance of the memory cell and propose an adequate system switching scheme.

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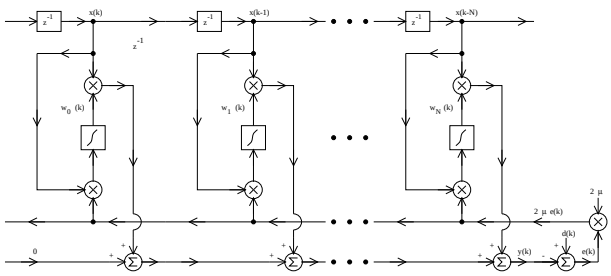

Fig. 1. Test system.

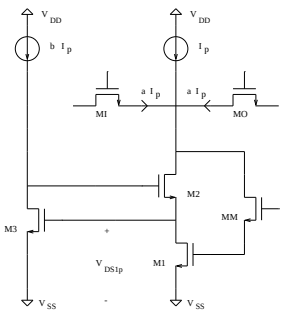

Fig. 2. Memory cell structure.

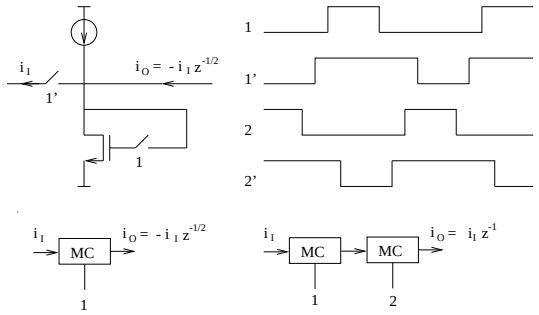

Fig. 3. SI delay cells.

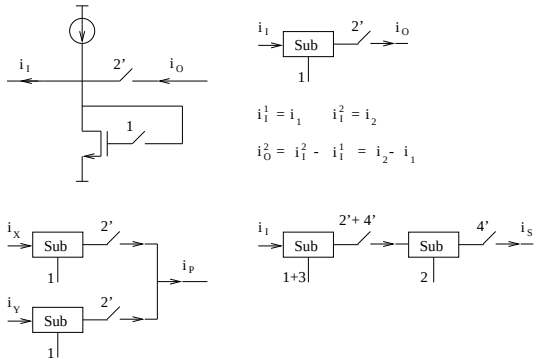

Fig. 4. SI subtractors.

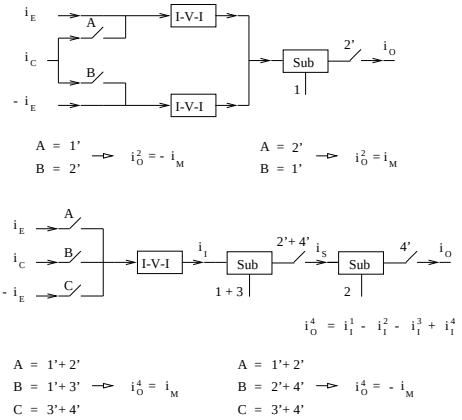

Fig. 5. Proposed SI four-quadrant multipliers.

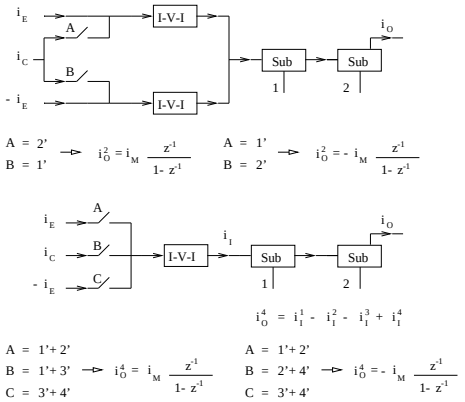

Fig. 6. Proposed SI multiplier-integrator cells.

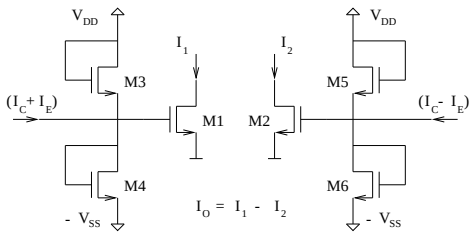

Fig. 7. Gain cell.

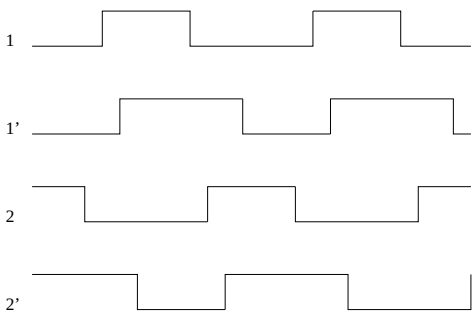

Fig. 8. Alternative switching sequence.

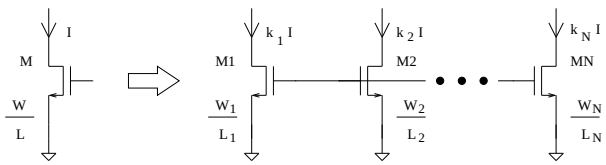

Fig. 9. Current replication.

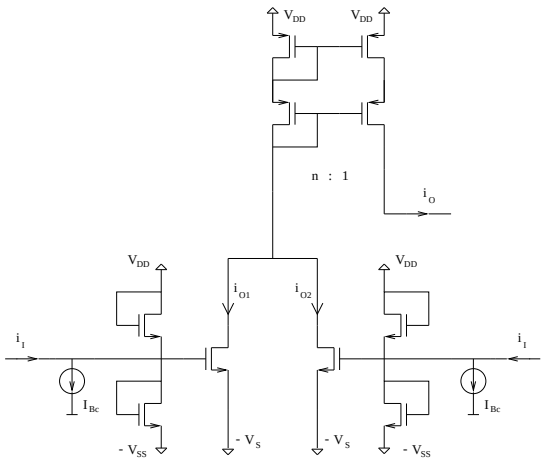

Fig. 10. Modified I-V-I converter.

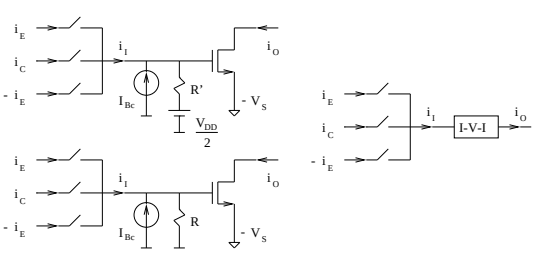

Fig. 11. Switched I-V-I converters.

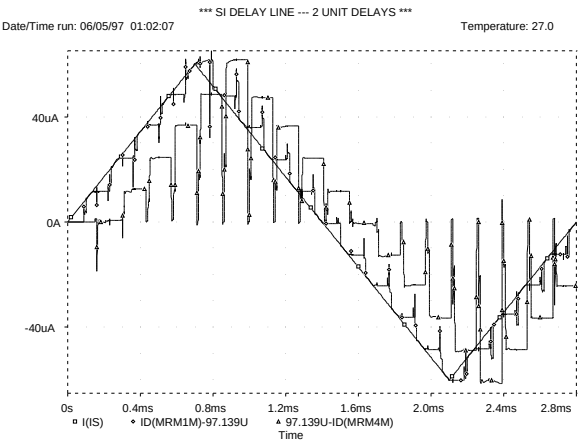

Fig. 12. Simulation results (delay).

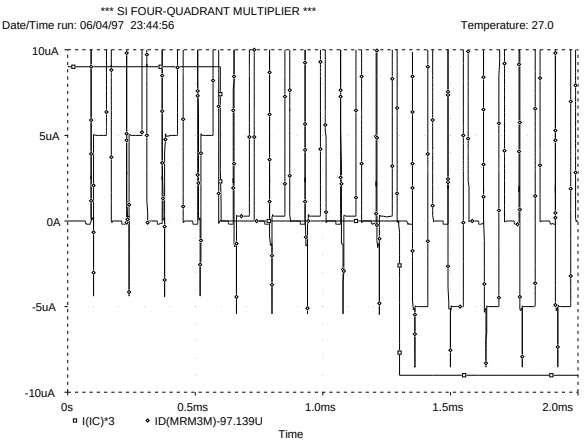

Fig. 13. Simulation results (multiplier).

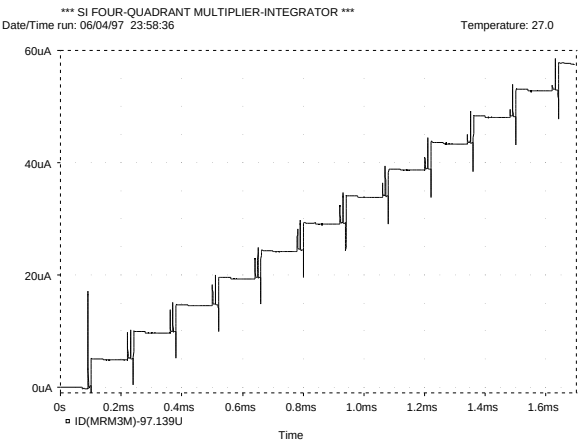

Fig. 14. Simulation results (multiplier-integrator).